WHAT IS CLAIMED IS:

1. A storage device control apparatus, comprising:

a channel controller which receives a data input/output request sent from an information processor to a storage device;

a disk controller which controls data input/output operations for the storage device; and

a cache memory which stores input/output data communicated between the channel controller and the disk controller, wherein

the channel controller comprises:

a communication interface unit which communicates with the information processor;

a data transfer unit connected via a first bus to the communication interface unit for transferring the input/output data communicated between the communication interface unit and the cache memory; and

a processor connected via a second bus to the data transfer unit for controlling the data transfer unit;

the communication interface unit transmits a read command to the data transfer unit, the read command indicating the processor to read data;

the data transfer unit sends, when the first bus conforms to a first communication protocol, a split response to the communication interface unit and sends

the read command to the processor, the split response indicating that readout data corresponding to the read command is transmitted later;

the data transfer unit does not send, when the first bus conforms to a second communication protocol, the split response to the communication interface unit and sends the read command to the processor;

the processor receives the read command, transmits the split response to the data transfer unit, and sends the readout data corresponding to the read command to the data transfer unit; and

the data transfer unit receives the readout data and sends the readout data to the communication interface unit.

2. A storage device control apparatus according to claim 1, wherein:

the first communication protocol is a PCI-X standard; and

the second communication protocol is a PCI standard.

3. A storage device control apparatus according to claim 1, wherein:

the data transfer unit includes a communication protocol setting unit which sets information indicating whether the communication protocol to which the first bus conforms is the first communication protocol or the second communication

protocol; and

the data transfer unit determines whether or not the split response is sent to the communication interface unit according to the information set to the communication protocol setting unit.

4. A storage device control apparatus according to claim 1, wherein:

the processor sends the read command to the data transfer unit, the read command accessing the communication interface unit;

the data transfer unit receive the read command, sends the split response to the processor, and sends the read command to the communication interface unit;

the communication interface unit sends the readout data corresponding to the read command to the data transfer unit; and

the data transfer unit receives the readout data and sends the readout data to the processor.

5. A storage device control apparatus according to claim 4, wherein:

the processor obtains a right to use the first bus and then sends the read command to the data transfer unit;

the processor receives the split response and releases the right to use the first bus; and

the data transfer unit obtains a right to use the first bus, sends the readout data to the processor,

and then releases the right to use the first bus.

6. A storage device control apparatus according to claim 1, wherein:

the channel controller includes a plurality of said communication interface units;

a first communication interface unit selected from the communication interface units is connected via the first bus to the data transfer unit;

the channel controller includes a third bus for connecting a second communication interface unit selected from the communication interface units to the data transfer unit;

the processor sends a first read command to the data transfer unit, the first read command accessing the first communication interface unit;

the data transfer unit receives the first read command, sends the split response to the processor, and sends the first read command to the first communication interface unit;

the processor sends a second read command to the data transfer unit, the second read command accessing the second communication interface unit;

the data transfer unit receives the second read command, sends the split response to the processor, and sends the second read command to the second communication interface unit;

the first communication interface unit sends first readout data corresponding to the first read

command to the data transfer unit;

the data transfer unit receives the first readout data and sends the first readout data to the processor;

the second communication interface unit sends second readout data corresponding to the second read command to the data transfer unit; and

the data transfer unit receives the second readout data and sends the second readout data to the processor.

7. A storage device control apparatus according to claim 1, wherein:

the channel controller includes a plurality of said communication interface units;

a first communication interface unit selected from the communication interface units is connected via the first bus to the data transfer unit;

the channel controller includes a third bus for connecting a second communication interface unit selected from the communication interface units to the data transfer unit;

the data transfer unit includes:

a first bus interface unit connected to the first bus for communicating data with the first communication interface unit;

a second bus interface unit connected to the second bus which communicates data with the processor; and

a third bus interface unit connected to the third bus for communicating data with the second communication interface unit;

the processor sends a first read command to the data transfer unit, the first read command accessing the first communication interface unit;

the second bus interface unit receives the first read command, sends the first read command to the first bus interface unit, and sends the split response to the first bus interface unit;

the first bus interface unit sends the first read command to the first communication interface unit;

the processor sends a second read command to the data transfer unit, the second read command accessing the second communication interface unit;

the second bus interface unit receives the second read command, sends the second read command to the third bus interface unit, and sends the split response to the processor;

the third bus interface unit sends the second read command to the second communication interface unit;

the first communication interface unit sends a first readout command corresponding to the first read command to the data transfer unit;

the first bus interface unit receives the first readout data, sends the first readout data to the second bus interface unit, and the second bus interface

unit sends the first readout data to the processor;

the second communication interface unit sends a second readout data corresponding to the second read command to the data transfer unit; and

the third bus interface unit receives the second readout data, sends the second readout data to the second bus interface unit, and the second bus interface unit sends the second readout data to the processor.

8. A storage device control apparatus according to claim 1, wherein:

the channel controller includes a plurality of said processors;

a first processor selected from the processors sends a first read command to the data transfer unit, the first read command accessing the communication interface unit;

a second processor selected from the processors sends a second read command to the data transfer unit, the second read command accessing the communication interface unit;

the data transfer unit receives the first and second read commands, sends the split response to the first and second processors, and sends the first read command to the communication interface unit;

the communication interface unit sends first readout data corresponding to the first read command to the data transfer unit;

the data transfer unit sends the first readout data to the first processor;

the communication interface unit sends second readout data corresponding to the second read command to the data transfer unit; and

the data transfer unit sends the second readout data to the second processor.

9. A storage device control apparatus according to claim 8, wherein the data transfer unit receives the first and second read commands and sends one of the first and second read commands which arrives first at the data transfer unit to the communication interface unit.

10. A storage device control apparatus according to claim 1, wherein:

the channel controller includes a plurality of said communication interface units and a plurality of said processors;

the channel controller includes:

a first bus for connecting a first communication interface unit selected from the communication interface units to the data transfer unit;

a second bus for connecting a first processor selected from the processors to the data transfer unit;

a third bus for connecting a second communication interface unit selected from the communication interface units to the data transfer

unit; and

a fourth bus for connecting a second processor selected from the processors to the data transfer unit;

the data transfer unit includes:

a first bus bridge connected to the first bus for communicating data with the first communication interface unit;

a second bus bridge connected to the second bus for communicating data with the first processor;

a third bus bridge connected to the third bus for communicating data with the second communication interface unit;

a fourth bus bridge connected to the fourth bus for communicating data with the second processor;

the second bus bridge is connected to the first and third bus bridges; and

the fourth bus bridge is connected to the first and third bus bridges.

11. A storage device control apparatus according to claim 10, wherein:

the first processor obtains a right to use the second bus and sends a first read command to the data transfer unit, the first read command indicating a data read operation to the first communication interface unit;

the second bus bridge receives the first read command, sends a first split response to the first

processor, and transfers the first read command to the first bus bridge;

the first processor receives the first split response and releases the right to use the second bus;

the first bus bridge receives the first read command and sends the first read command to the first communication interface unit;

the first processor obtains a right to use the first bus and sends a second read command to the data transfer unit, the second read command accessing the second communication interface unit;

the second bus bridge receives the second read command, sends a second split response to the first processor, and transfers the second read command to the third bus bridge;

the first processor receives the second split response and releases the right to use the first bus;

the first communication interface unit sends first readout data corresponding to the first read command to the data transfer unit;

the first bus bridge receives the first readout data and transfers the first readout data to the second bus bridge;

the second bus bridge obtains a right to use the first bus, sends the first readout data to the first processor, and releases the right to use the first bus;

the second communication interface unit sends

second readout data corresponding to the second read command to the data transfer unit;

the third bus bridge receives the second readout data and transfers the second readout data to the second bus bridge; and

the second bus bridge obtains a right to use the first bus and sends the second readout data to the first processor.

12. A storage device control apparatus according to claim 10, wherein:

the first processor sends a first read command to the data transfer unit, the first read command accessing the first communication interface unit;

the second processor sends a second read command to the data transfer unit, the second read command accessing the first communication interface unit;

the second bus bridge receives the first read command, transfers the first read command to the first bus bridge, and sends the split response to the first processor;

the first bus bridge receives the second read command and sends the second read command to the first communication interface unit;

the fourth bus bridge receives the second read command, transfers the second read command to the first bus bridge, and sends the split response to the

second processor;

the first bus bridge receives the second read command;

the first bus bridge receives first readout data corresponding to the first read command from the first communication interface unit and transfers the first readout data to the second bus bridge;

the first bus bridge sends the second readout data to the first communication interface unit;

the second bus bridge receives the first readout data and sends the first readout data to the first processor;

the first bus bridge receives second readout data corresponding to the second read command from the first communication interface unit and sends the second readout data to the fourth bus bridge; and

the fourth bus bridge sends the second readout data to the second processor.

13. A control method of controlling a storage device control apparatus, the storage device control apparatus comprising:

a channel controller for receiving a data input/output request sent from an information processor to a storage device;

a disk controller for controlling data input/output operations for the storage device; and

a cache memory for storing input/output data communicated between the channel controller and the

disk controller, wherein

the channel controller comprises:

a communication interface unit for communicating with the information processor;

a data transfer unit connected via a first bus to the communication interface unit for transferring the input/output data communicated between the communication interface unit and the cache memory; and

a processor connected via a second bus to the data transfer unit for controlling the data transfer unit, the control method comprising the steps of:

transmitting by the communication interface unit a read command to the data transfer unit, the read command indicating the processor to read data;

sending by the data transfer unit, when the first bus conforms to a first communication protocol, a split response to the communication interface unit and sending the read command to the processor, the split response indicating that readout data corresponding to the read command is transmitted later;

not sending by the data transfer unit, when the first bus conforms to a second communication protocol, the split response to the communication interface unit and sending the read command to the processor;

receiving by the processor the read command, transmits the split response to the data transfer unit,

and sending the readout data corresponding to the read command to the data transfer unit; and

receiving by the data transfer unit the readout data and sending the readout data to the communication interface unit.

14. A control method of controlling a storage device control apparatus according to claim 13, comprising the steps of:

sending by the processor the read command to the data transfer unit, the read command accessing the communication interface unit;

receiving by the data transfer unit the read command, sending the split response to the processor, and sending the read command to the communication interface unit;

sending by the communication interface unit the readout data corresponding to the read command to the data transfer unit; and

receiving the data transfer unit the readout data and sending the readout data to the processor.

15. A control method of controlling a storage device control apparatus according to claim 13, wherein:

the channel controller includes a plurality of said communication interface units;

a first communication interface unit selected from the communication interface units is connected via the first bus to the data transfer unit; and

the channel controller includes a third bus for connecting a second communication interface unit selected from the communication interface units to the data transfer unit, the control method comprising the steps of:

sending by the processor a first read command to the data transfer unit, the first read command accessing the first communication interface unit;

receiving by the data transfer unit the first read command, sending the split response to the processor, and sending the first read command to the first communication interface unit;

sending by the processor a second read command to the data transfer unit, the second read command accessing the second communication interface unit;

receiving by the data transfer unit the second read command, sending the split response to the processor, and sending the second read command to the second communication interface unit;

sending by the first communication interface unit first readout data corresponding to the first read command to the data transfer unit;

receiving by the data transfer unit the first readout data and sending the first readout data to the processor;

sending by the second communication interface unit second readout data corresponding to the second

read command to the data transfer unit; and

receiving the data transfer unit the second readout data and sending the second readout data to the processor.

16. A control method of controlling a storage device control apparatus according to claim 13, wherein:

the channel controller includes a plurality of said communication interface units;

a first communication interface unit selected from the communication interface units is connected via the first bus to the data transfer unit;

the channel controller includes a third bus for connecting a second communication interface unit selected from the communication interface units to the data transfer unit;

the data transfer unit includes:

a first bus interface unit connected to the first bus for communicating data with the first communication interface unit;

a second bus interface unit connected to the second bus for communicating data with the processor; and

a third bus interface unit connected to the third bus for communicating data with the second communication interface unit, the control method comprising the steps of:

sending by the processor a first read command

to the data transfer unit, the first read command accessing the first communication interface unit;

receiving by the second bus interface unit the first read command, sending the first read command to the first bus interface unit, and sending the split response to the first bus interface unit;

sending by the first bus interface unit the first read command to the first communication interface unit;

sending by the processor a second read command to the data transfer unit, the second read command accessing the second communication interface unit;

receiving by the second bus interface unit the second read command, sending the second read command to the third bus interface unit, and sending the split response to the processor;

sending by the third bus interface unit the second read command to the second communication interface unit;

sending by the first communication interface unit a first readout command corresponding to the first read command to the data transfer unit;

receiving by the first bus interface unit the first readout data, sending the first readout data to the second bus interface unit, and sending by the second bus interface unit the first readout data to the processor;

sending by the second communication interface unit a second readout data corresponding to the second read command to the data transfer unit; and

receiving by the third bus interface unit the second readout data, sending the second readout data to the second bus interface unit, and sending by the second bus interface unit the second readout data to the processor.

17. A control method of controlling a storage device control apparatus according to claim 13, wherein the channel controller includes a plurality of said processors, the control method, the control method comprising the steps of:

sending by a first processor selected from the processors a first read command to the data transfer unit, the first read command accessing the communication interface unit;

sending by a second processor selected from the processors a second read command to the data transfer unit, the second read command accessing the communication interface unit;

receiving by the data transfer unit the first and second read commands, sending the split response to the first and second processors, and sending the first read command to the communication interface unit;

sending by the communication interface unit first readout data corresponding to the first read command to the data transfer unit;

sending by the data transfer unit the first readout data to the first processor;

sending by the communication interface unit second readout data corresponding to the second read command to the data transfer unit; and

sending by the data transfer unit the second readout data to the second processor.

18. A control method of controlling a storage device control apparatus according to claim 17, comprising the steps of receiving by the data transfer unit the first and second read commands and sending one of the first and second commands which arrives first at the data transfer unit to the communication interface unit.

19. A control method of controlling a storage device control apparatus according to claim 13, wherein:

the channel controller includes a plurality of said communication interface units and a plurality of said processors;

the channel controller includes:

a first bus which connects a first communication interface unit selected from the communication interface units to the data transfer unit;

a second bus which connects a first processor selected from the processors to the data transfer unit;

a third bus which connects a second

communication interface unit selected from the communication interface units to the data transfer unit; and

a fourth bus which connects a second processor selected from the processors to the data transfer unit;

the data transfer unit includes:

a first bus bridge connected to the first bus for communicating data with the first communication interface unit;

a second bus bridge connected to the second bus for communicating data with the first processor;

a third bus bridge connected to the third bus for communicating data with the second communication interface unit;

a fourth bus bridge connected to the fourth bus for communicating data with the second processor;

the second bus bridge is connected to the first and third bus bridges; and

the fourth bus bridge is connected to the first and third bus bridges, the control method comprising the steps of:

obtaining by the first processor a right to use the second bus and sending a first read command to the data transfer unit, the first read command indicating a data read operation to the first communication interface unit;

receiving by the second bus bridge the first

read command, sending a first split response to the first processor, and transferring the first read command to the first bus bridge;

receiving by the first processor the first split response and releasing the right to use the first bus;

receiving by the first bus bridge the first read command and sending the first read command to the first communication interface unit;

obtaining by the first processor a right to use the first bus and sending a second read command to the data transfer unit, the second read command accessing the second communication interface unit;

receiving by the second bus bridge the second read command, sending a second split response to the first processor, and transferring the second read command to the third bus bridge;

receiving by the first processor the second split response and releasing the right to use the first bus;

sending by the first communication interface unit first readout data corresponding to the first read command to the data transfer unit;

receiving by the first bus bridge the first readout data and transferring the first readout data to the second bus bridge;

obtaining by the second bus bridge a right to use the first bus, sending the first readout data to

the first processor, and releasing the right to use the first bus;

sending by the second communication interface unit second readout data corresponding to the second read command to the data transfer unit;

receiving by the third bus bridge the second readout data and transferring the second readout data to the second bus bridge; and

obtaining by the second bus bridge a right to use the first bus and sending the second readout data to the first processor.

20. A control method of controlling a storage device control apparatus according to claim 13, wherein:

the channel controller includes a plurality of said communication interface units and a plurality of said processors;

the channel controller includes:

a first bus for connecting a first communication interface unit selected from the communication interface units to the data transfer unit;

a second bus for connecting a first processor selected from the processors to the data transfer unit;

a third bus for connecting a second communication interface unit selected from the communication interface units to the data transfer unit; and

a fourth bus for connecting a second processor selected from the processors to the data transfer unit;

the data transfer unit includes:

a first bus bridge connected to the first bus for communicating data with the first communication interface unit;

a second bus bridge connected to the second bus for communicating data with the first processor;

a third bus bridge connected to the third bus for communicating data with the second communication interface unit;

a fourth bus bridge connected to the fourth bus for communicating data with the second processor;

the second bus bridge is connected to the first and third bus bridges; and

the fourth bus bridge is connected to the first and third bus bridges, the control method comprising the steps of:

sending by the first processor a first read command to the data transfer unit, the first read command accessing the first communication interface unit;

sending by the second processor a second read command to the data transfer unit, the second read command accessing the first communication interface unit;

receiving by the second bus bridge the first

read command, transferring the first read command to the first bus bridge, and sending the split response to the first processor;

receiving by the first bus bridge the second read command and sending the second read command to the first communication interface unit;

receiving by the fourth bus bridge the second read command, transferring the second read command to the first bus bridge, and sending the split response to the second processor;

receiving by the first bus bridge the second read command;

receiving by the first bus bridge first readout data corresponding to the first read command from the first communication interface unit and transferring the first readout data to the second bus bridge;

sending by the first bus bridge the second readout data to the first communication interface unit;

receiving by the second bus bridge the first readout data and sending the first readout data to the first processor;

receiving by the first bus bridge second readout data corresponding to the second read command from the first communication interface unit and sending the second readout data to the fourth bus bridge; and

sending by the fourth bus bridge the second readout data to the second processor.